UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,151	09/22/2003	Vishnu K. Agarwal	M4065.0195/P195-B	5782

24998 7590 07/21/2005

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/665,151	AGARWAL ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,23,28,39,44 and 77-85* is/are pending in the application.

4a) Of the above claim(s) *4,7,12,14 and 15* is/are withdrawn from consideration.

5)☒ Claim(s) *84* is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-9,-11,13,23,28,39,44,77-83,and 85* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claims 82-83 and 85 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5, 6, 8, 9,11, 23, 28, 39, 44, 78-83 and 85 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al. [U.S. Pat. 6,037,216].

With respect to claim 1, Liu et al. (fig. 17, cols. 4-8) discloses a monolithic semiconductor device comprising:

a semiconductor substrate (1);

a plurality of upright free-standing microstructures (39) formed over the substrate (1); and

a brace (33) transversely extending between lateral sides of at least two of the free-standing microstructures (39).

With respect to claim 2, Liu et al. discloses that the brace (33) interconnects substantially all of the microstructures (see fig. 17).

With respect to claim 3, Liu et al. discloses that the brace (33) is located substantially near upper ends of the microstructures (39) (see fig. 17).

With respect to claim 5, Liu et al. discloses that the brace (33) comprises a microbridge structure extending above the substrate (1) and between two or more of the microstructures (39) (see fig. 17).

With respect to claim 6, Liu et al. discloses that the microstructures (39) each comprise a conductor material (see col. 6, lines 66-67 and col. 7, lines 1-14) portion standing upright over the substrate (1), and wherein the brace (33) interconnects the conductor material portion of two or more of the microstructures (39) (see fig. 17).

With respect to claim 8, Liu et al. discloses that the microstructures (39) comprise generally solid cylindrical shapes and the brace (33) comprises a microbridge structure (see fig. 17).

With respect to claim 9, Liu et al. discloses that the brace (33) comprises a dielectric material (see col. 6, lines 26-27).

With respect to claim 11, Liu et al. discloses that the wherein the microstructures (39) comprise conductive material (see col. 6, lines 66-67 and col. 7, lines 1-14) and the brace (33) comprises a dielectric (see col. 6, lines 26-27).

With respect to claim 13, Liu et al. discloses that the microstructures (39) are stud capacitors (see fig. 17).

With respect to claim 23, Liu et al. (fig. 17, cols. 4-8) discloses a semiconductor storage capacitor comprising:

a semiconductor substrate (1);

a plurality of upright free-standing capacitor storage node microstructures (39) formed over the substrate (1); and

a brace (33) transversely extending between lateral sides of at least two of the free-standing microstructures (39), wherein the microstructures comprise generally solid cylindrical shapes and the brace (33) comprises a microbridge structure.

With respect to claim 28, Liu et al. (fig. 17, cols. 4-8) discloses a semiconductor storage capacitor comprising:

a semiconductor substrate (1);

a plurality of upright free-standing capacitor storage node microstructures (39) formed over the substrate (1); and

a brace (33) transversely extending between lateral sides of at least two of the free-standing microstructures (39), wherein the microstructures comprise stud capacitors.

With respect to claim 39, Liu et al. (fig. 17, cols. 4-8) discloses a memory circuit, comprising:

a semiconductor substrate (1) having a memory cell including diffusion regions (13);

a dielectric layer (16) on the substrate (1);

conductive plugs (20) extending vertically from an upper surface of the dielectric layer (16) to respective diffusion regions (13);

a plurality of upright free-standing capacitor storage node microstructures (39) each formed over the dielectric layer (16) and a respective conductive plugs (20); and

a brace (33) transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures (39), wherein the microstructures (39) comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

With respect to claim 44, Liu et al. (fig. 17, cols. 4-8) discloses a memory circuit, comprising:

a semiconductor substrate (1) having a memory cell including diffusion regions (13);

a dielectric layer (16) on the substrate (1);

conductive plugs (20) extending vertically from an upper surface of the dielectric layer (16) to respective diffusion regions (13);

a plurality of upright free-standing capacitor storage node microstructures (39) each formed over the dielectric layer (16) and a respective conductive plugs (20); and

a brace (33) transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures (39), wherein the microstructures (39) comprise stud capacitors.

With respect to claim 78, Liu et al. (fig. 17, cols. 4-8) discloses a support structure on a semiconductor device comprising:

a plurality of braces (33) transversely extending between lateral sides of a plurality of microstructures (39) formed over a semiconductor substrate (1), wherein said plurality of braces (33) comprise a support structure for said plurality of microstructures (39).

With respect to claim 79, Liu et al. (fig. 17, cols. 4-8) discloses a brace for a semiconductor device comprising:

at least one brace (33) transversely extending between lateral sides of at least two of a plurality of microstructures (39) on a semiconductor substrate (1), wherein said at least two of said plurality of microstructures (39) are supported only by said at least one brace.

With respect to claim 80, Liu et al. (fig. 17, cols. 4-8) discloses an in-process semiconductor device comprising:

a semiconductor substrate (1);

a plurality of microstructures (39) formed over the substrate (1); and

at least one brace (33) transversely extending between lateral sides of at least two of said plurality of microstructures (39), wherein said at least two of said plurality of microstructures (39) are supported only by said at least one brace (33).

With respect to claim 81, Liu et al. (fig. 17, cols. 4-8) discloses a semiconductor support structure, comprising:

a semiconductor substrate (1);

a plurality of microstructures (39) formed over the substrate (1); and

at least one brace (33) transversely extending between lateral sides of at least two of said plurality of microstructures (39), wherein the brace (33) comprises a support structure.

With respect to claim 82, Liu et al. discloses that the at least one brace comprises a plurality of braces (32, 33) (see fig. 17).

With respect to claim 83, Liu et al. discloses that the plurality of braces (32, 33) form a lattice support structure (see fig. 17).

With respect to claim 85, Liu et al. (fig. 17, cols. 4-8) discloses a semiconductor storage capacitor comprising:

a semiconductor substrate (1);

a plurality of capacitor storage node microstructures (39) formed over the substrate (1), said microstructures (39) having vertical surfaces; and

a plurality of braces (32, 33) transversely extending between the vertical surfaces of the microstructures (39), the brace (32, 33) being located substantially near the upper ends of the vertical surfaces of the microstructures (39).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. [U.S. Pat. 6,037,216] in view of Findley [U.S. Pat. 6,243,653] newly cited.

With respect to claim 77, Liu et al. (fig. 17, cols. 4-8) discloses a memory circuit, comprising:

a semiconductor substrate (1) having a memory cell including diffusion regions (13);

a dielectric layer (16) on the substrate (1);

conductive plugs (20) extending vertically from an upper surface of the dielectric layer (16) to respective diffusion regions (13);

a plurality of upright free-standing capacitor storage node microstructures (39) each formed over the dielectric layer (16) and a respective conductive plugs (20); and

a brace (33) transversely extending between and laterally supporting respective lateral sides of at least two of the free-standing microstructures (39), wherein the microstructures (39) comprise stud capacitors.

Liu et al. discloses all the claimed limitation except a memory circuit fabricated on a semiconductor chip communicating with the processor. However, Findley shows that it is conventional for memory circuit (50) fabricated on a semiconductor chip communicating with the processor (48) (see figure 10, col. 5, lines 33-50). Therefore, it would have been obvious to the skilled in the art to include the processor with communicating with the memory circuit of the Liu et al. device for memory accessing.

Allowable Subject Matter

8. Claim 84 is allowed.

9. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

10. Applicant's arguments filed May 24, 2005 have been fully considered but they are not persuasive.

Applicant argues that Liu fails to teach or suggest "free-standing microstructures" or a "brace transversely extending between lateral sides of at least two of the free-standing microstructures".

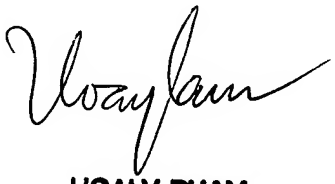
Applicant's arguments are not persuasive because Liu clearly discloses a plurality of upright free-standing microstructures (39) formed over the substrate (1) and a brace (33) transversely extending between lateral sides of at least two of the free-standing microstructures (39) (see fig. 17). Furthermore, the claim does not provide any specific meaning of the term "free-standing microstructures". Therefore, Liu clearly meets and anticipated the claim language.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



HOAI V. PHAM
PRIMARY EXAMINER